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Influence of Layout and Other Design Choices on the Performance of Large-Scale Photovoltaic Systems

By

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Influence of layout and other design choices on the performance of large-scale photovoltaic systems

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Abstract

The spatial layout of components in a photovoltaic system impacts the system's electrical performance. Therefore, it is important for designers to understand how to identify layouts that maximize power performance and best utilize land area, especially as the designed generation capacity and land area use for large-scale photovoltaic systems grows. Such identifications can be made through exploring multiple layout alternatives and comparing power output estimates; unfortunately, typical analysis methods and project schedules restrict—or do not facilitate—such investigations in engineering phases. This paper presents the analyses of power-related metrics for a range of typical layout strategies, block sizes, and other related engineering considerations for large-scale photovoltaic systems. The goal is to further communicate the influence of layout considerations and to identify trends, which—although may not hold for every system design—can be used to guide layout optimization explorations.

Keywords-Large scale Photovoltaic; Design strategies; Layout optimization

1. Introduction

The quantity and designed generation capacities of large-scale photovoltaic (PV) systems have increased rapidly over the past decade, influenced greatly by the steadily decreasing costs of its core components, i.e., PV modules (Solarbuzz.com, 2012b). As a result, these systems have become a hot topic for discussion, spurring many explorations into the nuances involved in their realization and operation. From an electrical engineering perspective, researchers have investigated the characteristics of these systems (e.g., Curtright, 2008), studied the potential safety

hazards (e.g., Hastings, 2011), and developed calculation models to analyze system designs (e.g., Yuventi, 2012a). The results of such studies and the lessons learnt during installation and operation for PV and other power systems are—and will be—eventually used to create building codes and engineering guidelines. Electrical construction engineers use these guidelines to design the systems and perform any analyses that are required by the applicable regulatory agencies or system operator.

Although popular codes or engineering guidelines—such as the National Electrical Code (NEC), which governs electrical construction in the U.S.—discuss design considerations, they do not explicitly communicate the impact that spatial layout and interconnection schema in PV systems. This is unfortunate since studies indicate that there are correlations between these design choices and the estimated system performance, costs, and reliability (Yuventi, 2012b). Since these relationships are not communicated in the codes, it is unlikely that engineers will perform the additional analyses needed to explore layout-related alternatives that can potentially create design optimization strategies, etc. In addition, the quick development cycles used in most projects further restricts such explorations in the engineering phase (Yuventi, 2013). This is a concern now, and may become a limitation in the future as the land area use of these systems increase, since designers may not know how to balance land use and performance expectations.

This paper aims to further convey the relationship between layout and performance by expanding the analysis presented in (Yuventi, 2012b) to include a variety of system sizes, typical layouts, and other related considerations. Here the term 'layout' is used to represent the spatial layout and electrical interconnections of the functional electrical components and subsystems. The goal is not to explicitly recommend that a specific strategy should be used in all projects but to illustrate the influence of layout on performance and potentially guide the exploration of layout-related or help designers select from a set of design alternatives. To begin this discussion, I start with a functional description of typical utility-run grid-connected large-scale PV systems and identify some of the key design choices.

2. Electrical components in large-scale photovoltaic systems

A PV system can be divided into two networks: the direct current (DC) network or 'DC power block' and the alternating current (AC) network (Yuventi, 2012a). Electricity is generated in the DC power block by PV modules in the form of DC power and transmitted via a circuitry of electrical wiring and protection devices—such as fuses—to an inverter, which converts it to AC power. Larger systems often use combiner boxes to merge multiple DC power channels to consolidate wiring and fuses and to accommodate for limited input connections at the inverter. Some systems may also use storage devices—such as batteries—in DC power blocks to store any excess electrical energy. In the AC network, the AC power is transmitted via more wiring, protection devices—such as circuit breakers—and service panels until it reaches it point of use, which is a utility connection in most PV systems. The components and connection schemes in AC networks are more project specific than DC power block components, which are easier to generalize. As a result, the focus of this discussion is on the electrical aspects of the DC power block.

I define large-scale PV as systems with total designed maximum DC power output of atleast 1MW. Such systems often have multiple DC power blocks and can cover many hectares of land (Wolfe, 2012), the majority of which is occupied by the DC power blocks, or more specifically, the PV modules. The designed generation capacity of each block and the total number of blocks are functions of the number and type of inverters that are used. For example, a 10MW system that uses twenty 500kW inverters will likely have 20 DC power blocks, each with a designed maximum DC power generation close to 500kW, since that is the maximum power that the inverters can facilitate. This maximum represents the 'block size' of the DC power block. In some systems, multiple inverters are integrated—spatially and electrically—to act as single inverter serving a block. In these cases the effective block size can be viewed as the sum of the capacity of the integrated inverters.

Typical DC power blocks consist of many modules and, usually, the same type of module is used throughout the block, i.e., all modules are the same manufacturer

model and have similar characteristics. Modules are normally connected in series into 'module-strings' in order to increase the operating voltage of the DC power block. All of the module-strings in a block should have the same number of modules. Multiple module-strings are connected in parallel to a combiner box; multiple combiner boxes are connected in parallel to an inverter; and multiple inverters may be connected in parallel to an AC service panel, as illustrated in Figure 1 (ignoring AC elements). In this figure and in the remainder of this paper, *z* represents the number of modules in a module-string, *n* represents the number of module-strings connected to a combiner box, *x* represents the number of combiner boxes connected to an inverter, and *y* represents the number of DC power blocks in the system. Modules are denoted as $P_{\#}$, module-strings as $M_{\#c\#}$, combiner boxes as $C_{\#}$, and inverters as $Inv_{\#}$. Wiring between module-strings is denoted as W_m and between combiner boxes and inverters as W_c. It is important to note that each interconnection consists of at least two conductive wires: a forward path or positive wire and a return path or negative wire (the negative paths can be combined in the case of thin-film PV modules, however this case it not considered in this analysis).

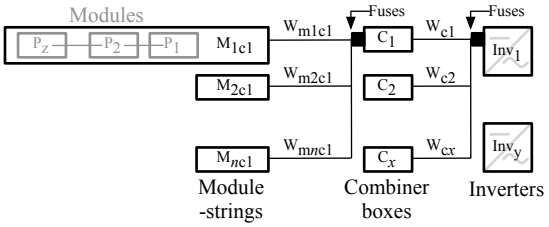

Figure 1. Interconnections between DC power components

2.1 Realization factors

Realizing a large-scale PV system involves many considerations, including: desired power output; site characteristics such as land dimensions and location; cost of construction and/or operation, etc. Specific to this discussion, these considerations impact various DC power block design choices, including the characteristics of wiring, and the selections for the variables *x*, *y*, *z*, and *n*. These choices are inter-related, especially in code-based systems, such as systems that conform to NEC—which is the case for most U.S. systems. Also, based on most design strategies, these choices are directly related to spatial layout in the DC power blocks.

2.2 Spatial layout considerations

Layout considerations range from the arrangement of modules in module-strings to the arrangement of DC power blocks on the site. Figure 2 illustrates example module-string configurations—"Loop" and "Straight" arrangement—that are used in the analyses presented later in this paper. In this figure and throughout this discussion, d_{Lpv} and d_{Wpv} represents the length and width of the modules and d_{Lm} represents the length of the module-string. Figure 3 illustrates a typical layout strategy for module-strings and combiner boxes in a DC power block, wherein module-strings are arranged into rows with the corresponding combiner box at one end. The distance d_c represents the approximate spacing between each row (to provide walking paths) and d_{Ldc} and d_{Wdc} approximate the length and width of the DC power block footprint. In large systems, it is common for all combiner boxes to have the same n, therefore, all rows are approximately the same length and the product $n{\cdot}x$ captures the total number of module-strings in the block. It is also common for all d_c to be the same and, as a result, the selections for n and x can dictate the dimensions of the block's land area footprint. Also, these selections dictate the lengths of wires. Module-strings farthest away from the combiner box have the longest wires, i.e., W_{mnc1} is longer than W_{m1c1} and likewise the combiner boxes farthest from the inverter have the longest W_c.

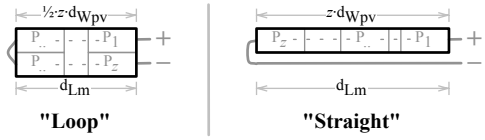

Figure 2. Example of modules in module-strings

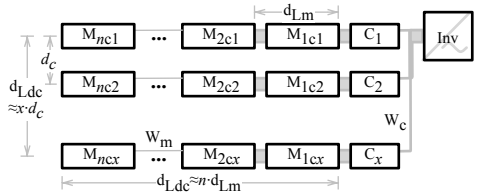

Figure 3. Example DC power block layout

It is common for all or most of the blocks in a large-scale system to be identical, in designed-performance and dimensions; although some variations may

exist due to various conditions such as soil characteristics, foliage, land slope, etc. As an example, a system divided into four DC power blocks can be arranged as illustrated in Figure 4, where 'DCA' and 'DCB' are DC power blocks with the same designed block size but with different dimensions. The motivation for this study is to determine whether designers should choose DCA over DCB, based on the performance of the individual DC power blocks. Also within each block, it will be helpful to know the advantages and disadvantages of a set of layout alternative strategies, such as those shown in Figure 5.

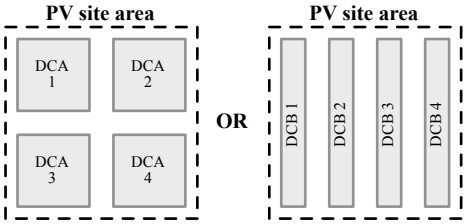

Figure 4. Example site layouts

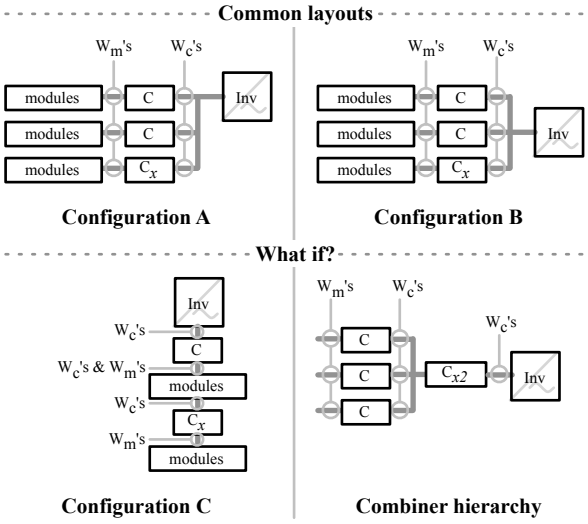

Figure 5. Alternative DC power block layout strategies

3. Layout-performance analyses

Previous studies (Yuventi, 2012b) have illustrated relationships between layout and performance using 1MW power blocks based on Configuration A in Figure 5 and the "Loop" module-string arrangement using 100% International Annealed Copper Standard (IACS)-rated copper (Cu) wires. In these studies, *n* and *x* that resulted to

approximately square block area footprints also maximized the power output of the block at the standard testing conditions (STC) of the modules. This paper expands that analysis to include different block sizes, the layout configurations, 63%IACS aluminum (Al) wiring, and non-STC operation.

3.1 Simulation setup

The maximum DC power available at the inverter P_{inv} was determined for the various design alternatives and conditions using a method that mimics ideal maximum power point (MMP) inverter tracking behavior and accounts for DC power losses due to wiring (Yuventi, 2012a). The simulated designs consisted of module-strings of twenty PV modules, each module having the STC characteristics shown in Table 1, where STC represents an irradiance Ir_{STC} of 1000Wm^{-2} and an ambient temperature of 25°C. It was assumed that all of the modules in the system were exposed to the same conditions. Appendix A presents the equations used to adjust the STC characteristics for other temperatures and irradiances. The wires were sized based on the NEC minimum requirements and the resistances were calculated based on provisions in the 2011 NEC handbook (Early, 2010) to mimic a typical engineering process for U.S. projects. Appendix B presents more information on wiring considerations and resistance calculations.

Table 1. 225W PV module characteristics

Electrical characteristics at STC	
Maximum power output (P_{mp})	225W
Voltage at power output (V_{mp})	30V
Current at Power output (I_{mp})	7.5A
Open-circuit voltage (V_{oc})	38V
Short-circuit current (I_{sc})	8.0A
Temperature characteristics	
Temperature coefficient of V_{oc} (k_{Voc})	-0.4%/°C
Temperature coefficient of I_{sc} (k_{Isc})	-0.05%/°C
Mechanical characteristics	
Dimensions (d_{Lpv} x d_{Wpv})	1.5 x 0.75 m

3.2 Simulated design variants

The layouts shown Figure 5 and the module-string arrangements shown in Figure 2 were simulated for block sizes ranging from 100kW to 10MW. Each of the simulated designs had spatial characteristics similar to that shown in Figure 3, with d_c=5m, 1m between the closest module-string to the corresponding combiner box—e.g., between M_{1c1} and C_1—and 2m between the closest combiner box to the inverter—e.g., between C_1 and the inverter. The module dimensions shown in Table 1 resulted in d_{Lm}=7.5m and d_{Lm}=15m for the Loop and Straight module-string arrangements respectively. The number of module-strings in each block size was chosen so that the ideal power output P_{inv_ideal}, i.e., the power at the inverter if the wires had no resistance, is slightly above the block size, where

$$P_{inv\_ideal} = z \cdot n \cdot x \cdot \mathrm{P_{mp}}. \quad (1)$$

To further structure the analyses, multiples of 24 were chosen to allow for a wide range of *x*:*n* ratios. Values for *n* and *x* were chosen so that the quotient *x/n* was $0.10 \leq x/n \leq 25$ to limit the analysis to practical ranges. For example, for the 100kW block size—where P_{inv_ideal}=108kW—the simulated *x*:*n* ratios were: 12:2 (6), 8:3 (2.667), 6:4 (1.5), 4:6 (0.667), 3:8 (0.375), and 2:12 (0.167). It was assumed that the combiner boxes allow for an unlimited number of inputs.

4. Simulation results

Figures 6, 7 and 8 capture some of the results of the simulations. Configuration A consistently had the lowest P_{inv} for all considerations, i.e., *x:n* or *x/n*, block size, material, temperature, etc. Configuration B provided the highest P_{inv} as *x/n* increased, i.e., as the number of combiner boxes got significantly larger than the number of module-strings per box. Configuration C allowed for the highest P_{inv} with each block size, however, although it consistently outperformed Configuration A; it only performed better than Configuration B at low *x/n* values, as shown in Figure 6.

The simulations indicated that there was a certain range for *x:n* or *x/n* that maximized P_{inv} for each block size dependent upon the module-string configuration.

This is especially seen in Configuration A, where, in STC simulations, *x/n* values close to 1.5 and 3 resulted in the highest P_{inv} for the Loop and Straight module-string arrangements respectively. These results support previous studies, which indicate that square layouts maximize performance (Yuventi, 2012b). That is, if "*Squareness*" is used to quantify the geometry of a layout, and

$$Squareness = \frac{\mathrm{d_{Ldc}}}{\mathrm{d_{Wdc}}} \cong \frac{n}{x} \cdot \frac{\mathrm{d_{Lm}}}{\mathrm{d_c}}, \qquad (2)$$

then for the Loop arrangement, as $x/n \rightarrow 1.5$, then $Squareness \rightarrow 1$ and as $n/x \rightarrow 3$, then $Squareness \rightarrow 1$ for the Straight arrangement. However, *Squareness* close to 1 did not always maximize P_{inv} for all of the layout configurations and other conditions simulated. In particular, the *x/n* for best P_{inv} varied based on block size and nominal temperature for a given layout, as illustrated in Figure 7 (differing irradiances did not change the ideal *x/n* values). However, the results show that *x/n* in the 1 to 4 range resulted maximum or near maximum P_{inv} the majority of the time.

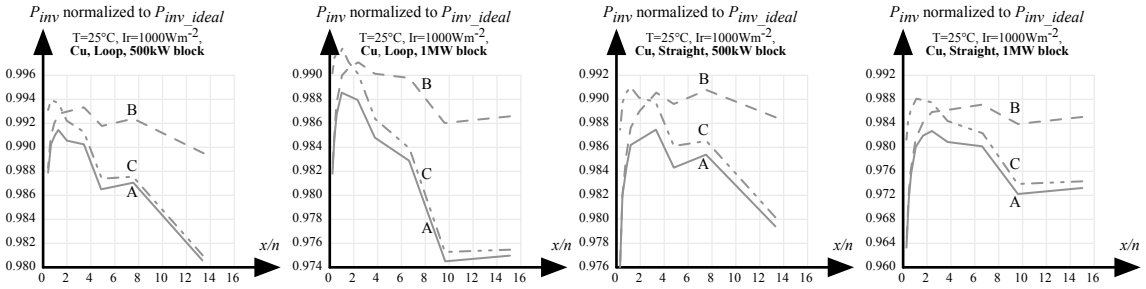

Figure 6. Configuration A was consistently outperformed by Configurations B and C, with B winning for high *x/n* and C wining for low *x/n* and resulting in best overall output.

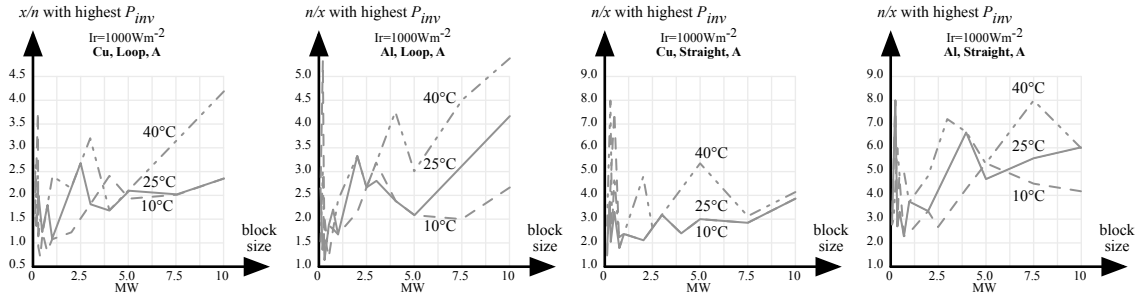

Figure 7. *x/n* that maximizes P_{inv} varies based on block size and expected temperatures.

Copper wiring always resulted in higher P_{inv} than aluminum—by having lesser power loss due to electrical resistance. However, regardless of the wire

material or configuration used, the wiring power losses increased steadily with increasing block size, as shown in Figure 8. In addition, the Loop module-string arrangement always outperformed the Straight arrangement since it the lengths of W_m in the Loop arrangement were half that of the corresponding W_m in the Straight arrangement, and hence having half the electrical resistance.

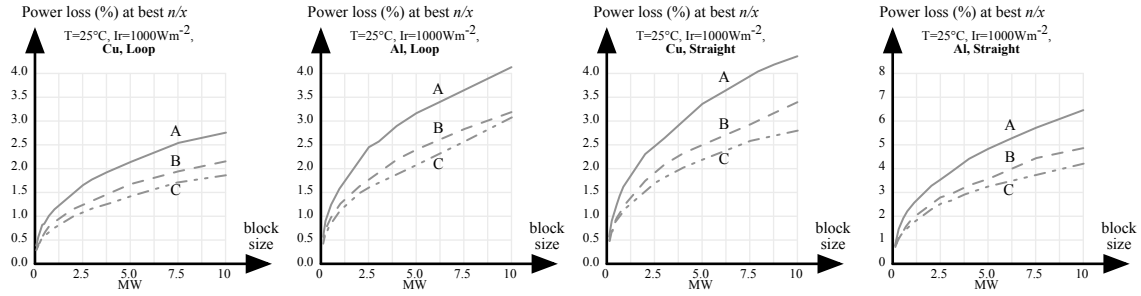

Figure 8. Copper consistently outperformed aluminum and Loop always outperformed Straight.

4.1 Cost considerations

Engineers are often sheltered from detailed project cost considerations. However, in many cases it is important for them understand how their design choices and optimization strategies may impact critical project cost considerations. This is certainly the case for the layout considerations addressed in this paper being that studies have demonstrated that certain *n* and *x* selections can minimize construction costs in DC power blocks (Yuventi, 2012b). Cost-to-power performance (*$/W*) is a popular evaluation metric for large-scale PV construction projects. Costs typically capture material and labor costs involved in construction and power performance represents the power output of the system or individual blocks. The common goal is to minimize this metric, i.e., have a higher performing system at lower costs. PV modules can account for 70-80% of construction costs in grid-connected PV systems (Tan, 2012). Since these costs are independent of layout considerations—i.e., number of modules is constant for a given block size—the influence of layout on *$/W* evaluations may not be too visible. However, if the trends of decreasing module prices (Solarbuzz.com, 2012b) and rising material costs associated with electrical wiring (Yuventi, 2012b) continue, then the influence of wiring and—by association—layout will become more significant in *$/W* analyses.

To explicitly convey the influence of layout on cost-to-performance analyses I define a term "cost of electrical layout-to-P_{inv}" ($\$_{layout}/P_{inv}$) for a DC power block. In this metric, $\$_{layout}$ captures the total material and labor costs associated with DC wiring, conduits, fuses, and combiner boxes based on 2012 average cost data for U.S. projects (Charest, 2011). (Wiring and conduit costs are typically in cost-per-unit length.) The costs associated with conduit elbows and wire connectors were ignored because they represent insignificant portions of these layout costs. $\$_{layout}/P_{inv}$ evaluations were made for all of the simulated design variants and conditions. Similar to the P_{inv} evaluations, these result suggested x/n values in the 1 to 4 range minimized or resulted in near minimum $\$_{layout}/P_{inv}$, especially for Configuration A and C, as illustrated in Figure 9. Also like the P_{inv}, this range is dependent on module-string arrangement, wire material and slightly dependent on evaluated temperature. The x/n values that resulted in the smallest $\$_{layout}/P_{inv}$ for each block size were in most cases largest for Configuration B and smallest for Configuration C. Also, even though copper wiring can be twice as expensive as aluminum, copper resulted in lower $\$_{layout}/P_{inv}$ due the larger power losses incurred with aluminum.

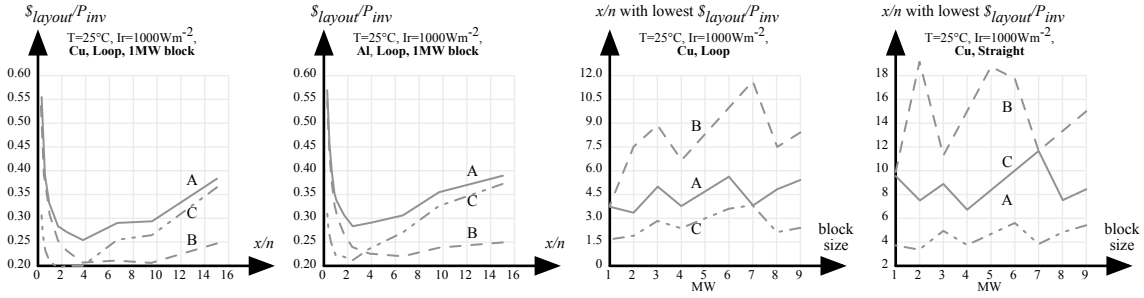

Figure 9. A range for x/n minimized $\$_{layout}/P_{inv}$, in addition, copper wiring results in lower $\$_{layout}/P_{inv}$ than aluminum even though copper is more expensive.

4.2 Combiner box hierarchies

Two-level combiner box hierarchies—as illustrated in Figure 5—were simulated for the Configuration B layout to determine if there will be any performance or cost-to-performance advantages. With x_2 representing the total number of combiner-box parents—i.e., the combiner boxes directly connected to the inverter—and x representing the original number of combiners that are directly connected to

module-string, the simulations were performed for x_2:x ratios of 1:2, 1:3, and 1:6 on layouts with x:n ratios that resulted in x being multiples of 6. It was assumed that there were at least 2m between the closest combiner-box and combiner-box parent, and 2m between the combiner-box parent and the inverter.

The simulation results indicated that hierarchies only outperformed normal layout when x/n is large, as illustrated in Figure 10. In most cases this superior performance started at the point when x/n is larger that the x/n value that allows for the best P_{inv} in the normal layout. However, combiner box hierarchies resulted in worse, i.e., higher $\$_{layout}/P_{inv}$ than the normal layout since the additional costs associated with combiner-box hierarchies, i.e., the additions wiring, fuses, combiner boxes, etc., outweighed the increased P_{inv}.

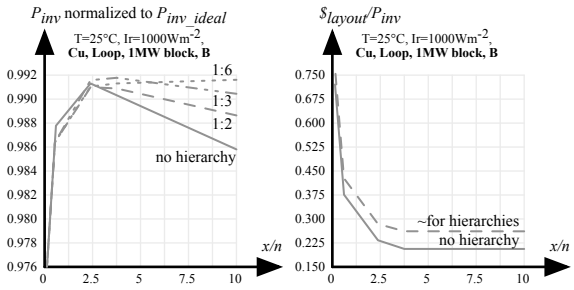

Figure 10. Combiner box hierarchies work for large x/n but are always more costly.

5. Insights from simulations

The simulation results indicate that there are relationships between layout, power, and costs, in a large-scale PV system. The 'ideal' layout considerations, e.g., x/n values, can vary based on known or measurable conditions, such as block size and temperature. However, the results encourage the following general inferences:

- Having $1 \leq x/n \leq 4$ will likely result in the best of near-best performances.
- Selecting DC power block layouts that decrease total wiring lengths will increase power and reduce cost-to-performance.

Therefore, in reference to Figure 4, DCB is most likely better than DCA in power output and cost-to-performance evaluations. Also, Configurations B and C always

outperform Configuration A and the Loop module-string arrangement always outperforms the Straight arrangement.

The resistance of the interconnection wiring in DC power blocks is the underlying reason why layout has an influence on performance. The inferences presented are driven by the assumption that all similarly functioning wires are the same size—that is the same sized wires are used for all W_m and the same sized wires are used for all W_c—which is common practice in U.S.-based projects (Yuventi, 2013). As a result, the operating points of modules and the power that they contribute at the inverter are functions of wire length; with longer lengths resulting in lesser power contributions (Yuventi, 2012a; Yuventi, 2012b). To counteract decreased performance due to layout constraints, designers can choose to use less resistive wires, e.g., copper instead of aluminum, larger wire size, or experiment with other wire-size-related techniques, such as a Resistance Matching (Yuventi, 2012b; Yuventi, 2013). However, these choices are likely to increase system costs and may not be justifiable in cost-to-performance evaluations (Yuventi, 2012b).

The discussions and recommendations presented focuses on the DC power blocks. As stated, there are normally multiple blocks in a large-scale PV system. The layout of these blocks on the site impact the total power output of the system, i.e., the power available at the grid-connection for on-grid systems, by influencing the lengths of wiring in the AC-power network. Fortunately, there are typically more components—especially wiring—in the DC power blocks than in the AC power distribution. The AC wiring are normally larger in size, and as a result have smaller resistances-per-unit length (see Appendix B), and AC voltage transformations can be used to reduce power losses for longer runs, which is not possible within the DC power blocks. Therefore the impact of layout, and the costs and engineering associated with optimizing AC-power network layout considerations are likely to be not as significant or demanding as considerations within the DC power blocks.

6. Conclusions

It is important for large-scale PV system designers to understand how choices related to layout can impact system performance in order to structure design approaches and/or select from design alternatives. This work attempted to develop this understanding by analyzing a number of common layout strategies and other engineering considerations for typical building code-governed systems to identify trends related to the power output of DC power blocks. Ideally the understandings developed should be reinforced on a project-by-project basis by conducting performance-based simulation—similar to those discussed in this paper—taking into account the specifics of the project, e.g., module characteristics, etc. However, if time does not permit this exploration, and/or to focus this exploration, the results of this analysis suggests that DC power block with squarer footprint areas are almost always better than those with elongated areas in both performance and cost-to-performance. Also, layouts that minimize wire lengths are always better for both of these considerations. Lastly, implementing combiner box-hierarchies can be used to improve power output for layouts with high x/n values, however the improved power output may not justify the additional costs.

Acknowledgment

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Appendix A: Calculation models

The relationship between current and voltage for the PV modules was captured using a piece-wise *I-V* model that produces I-V curves that are very similar to the typical curve provided by module manufacturers (Yuventi, 2012a). Examples of the derived curves are illustrated in Figure A-1 for the module information provided in Table 1. Adjustments for temperatures and irradiances other than that of STC were made using Eq. (A.1)-(A.3) where T represents the ambient temperature.

$$I_{mp} = I_{mp\_STC} \cdot \left(\frac{Ir_{actual}}{Ir_{STC}}\right), \quad (A.1)$$

$$I_{sc} = I_{sc\_STC} \cdot \left(\frac{Ir_{actual}}{Ir_{STC}}\right) \cdot [1 + k_{Isc} \cdot (T_{actual} - T_{STC})], \quad (A.2)$$

$$V_{oc} = V_{oc\_STC} \cdot [1 + k_{Vsc} \cdot (T_{actual} - T_{STC})]. \quad (A.3)$$

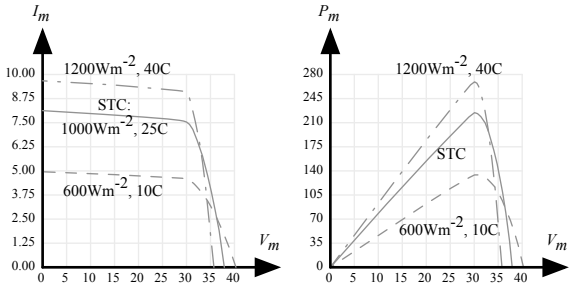

Figure A-1. Calculated *I-V* curve for the modules

An iterative calculation method and MPP tracking algorithm described in (Yuventi, 2012a) was used to estimate P_{inv} in the simulations. This method was originally based on layouts that do not have combiner-box hierarchies. In order to analyze these hierarchies slight, logical adjustments were made to the method as shown in Figure A-2.

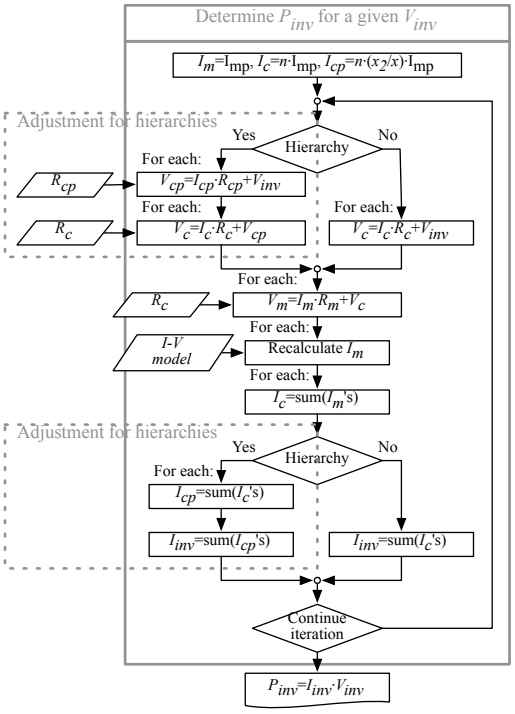

Figure A-2. Adjustments to the Iteration calculation method for combiner box hierarchies.

Appendix B: NEC wire sizes, conduits, and fuses

The NEC mandates that the current carrying capacity of W_m be 56% greater than the short-circuit current of the modules or module-strings, i.e., $>1.56 \bullet I_{sc}$ (Earley, 2010). Likewise, W_c wiring has to have a capacity 56% greater than the total shore-circuit current possible on the corresponding interconnection, i.e., $>1.56 \bullet n \bullet I_{sc}$. The current carrying capacity of wires depends on the conducting material used, the temperature rating of the wire insulation, and the wire size.

Wire sizes are measured in American Wire Gauge (AWG) or circular-mils (kcmil) proportional diameter of the conducting material. Smaller AWG and larger kcmil correspond to larger corresponding wire sizes. The NEC presents the minimum size for wires that can be used given the desired current carrying capacity, conducting material, and insulation type. It is common for electrical construction initiatives to attempt to use these NEC minima unless there are other limiting circumstances. Therefore NEC minima were used in the simulated designs and 12AWG wires were the smallest gage used to conform to most U.S. jurisdictions. All of the W_m wiring in the simulated designs were stranded 12AWG and W_c sizes ranged from stranded 12AWG to 600kcmil sized based on the provisions made in Article 310.15(B) of the 2011 NEC (Earley, 2010) using 60°C and 75°C rated conductors. W_c sizes were limited to 600kcmil because material and labor costs typically increase rapidly for wire sizes above 600kcmil and as a result contractors rarely use these larger sizes. Also, it was assumed that the wires were in conduits run on trays or on the earth's surface—with the positive and negative leads in the same conduit—so that no de-rating was necessary. Table B-1 illustrates some of the W_c wire sizes used as a based on the corresponding n (or x_2/x for combiner box hierarchies). This table also shows the corresponding DC resistances, measured in ohms per kilometer (Ω/km) and approximate current carrying capacity at 25°C ambient temperature respectively derived from the Chapter 9-Table 8 and Article 310.15(B) of the 2011 NEC (Earley, 2010). These values were used to determine the resistance of the interconnections, making sure to account for both the positive and negative leads. Resistance and power losses within module-strings and fuses were

ignored since they do not contribute to this comparative analysis. For cost evaluations, the fuse sizes were determined based on Article 690.8 (B)(1)(c) of the NEC and priced based on 2012 average cost data for U.S. projects (Charest, 2011).

Table B-1. W_c sizes based on *n* assuming 25°C ambient temperature

n or x_1/x	2	10	50	100
$1.56 \bullet n \bullet I_{sc}$	24.96A	124.8A	624A	1248A
Cu size	12AWG	1AWG	2x350kcmil	3x600kcmil
Ω/km	6.50	0.505	0.06025	0.023467
Max *I*	26.25A	136.5	651A	1323A
Al size	10AWG	1/0AWG	2x500kcmil	4x500kcmil
Ω/m	6.679	0.660	0.06955	0.034775
Max *I*	26.25A	126A	651A	1302A

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