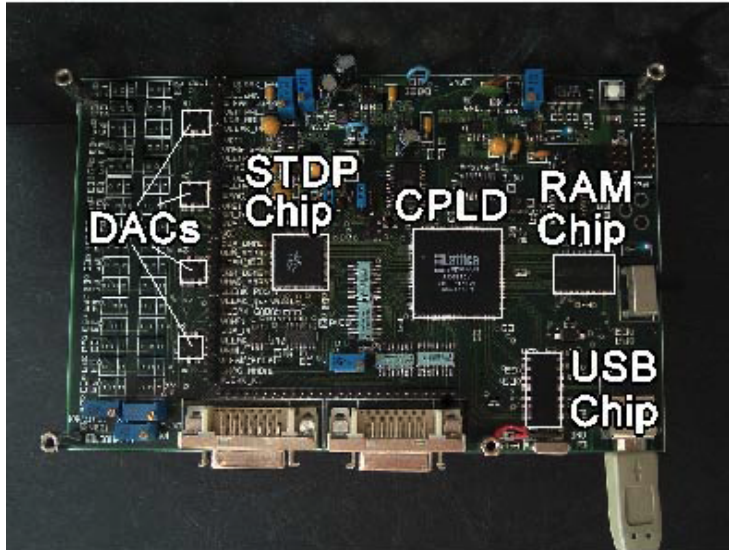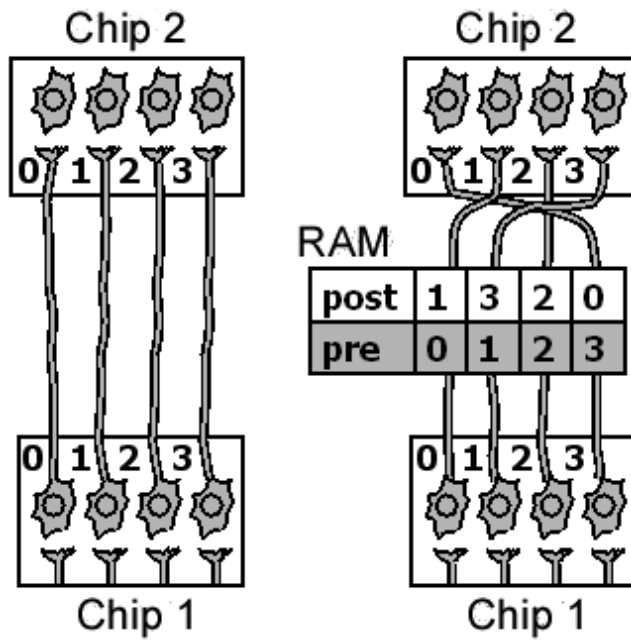# The Hardware

DACs and RAM specify properties & connectivity of STDP chip's 1280 silicon neurons.

Computation is analog; communication is digital.
Spikes share a common set of input/output lines.
Addresses identity of source/target.

Address-event representation
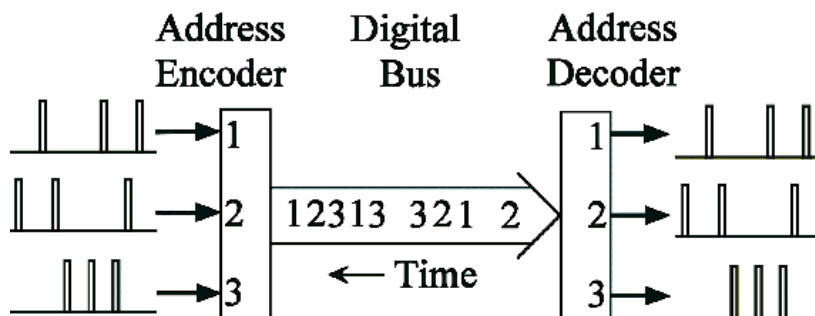

A neuron's address is output when it spikes; the corresponding synapse is activated.

Assigning unique addresses to N sources/targets requires $\text{Log}_2[N]$ bits—10 bits for 1024 neurons.

These bits are transmitted over $\text{Log}_2[N]$ shared wires—have to run N times faster.

Source–target pairs are specified by a look-up table (stored in RAM).

Address-event link

Encoder outputs source's address; decoder recreates spike at target location.

The encoder's N inputs are tied to the neurons' spike-outputs; it places $\text{Log}_2[N]$-bit addresses on the bus.

The decoder's $\text{Log}_2[N]$ inputs come from the bus; its N spike-outputs trigger postsynaptic potentials.

Dealing with coincidences
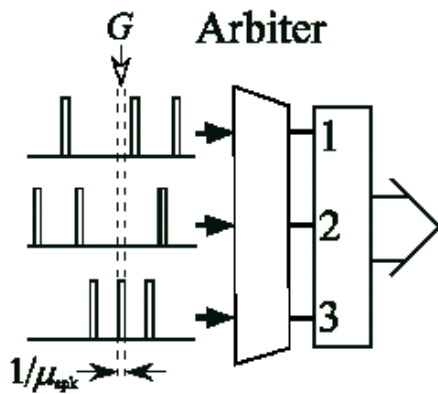
An arbiter ensures the encoder's inputs are activated one at a time.

If two neurons fire at the same time, the arbiter selects one of them. That neuron's spike is transmitted first, and then the second neuron's spike is transmitted. The delay is negligible: 40ns for a (typical) bus that transmits $\mu_{\text{spk}} = 25\,\text{M}$ addresses/sec.

STDP chip
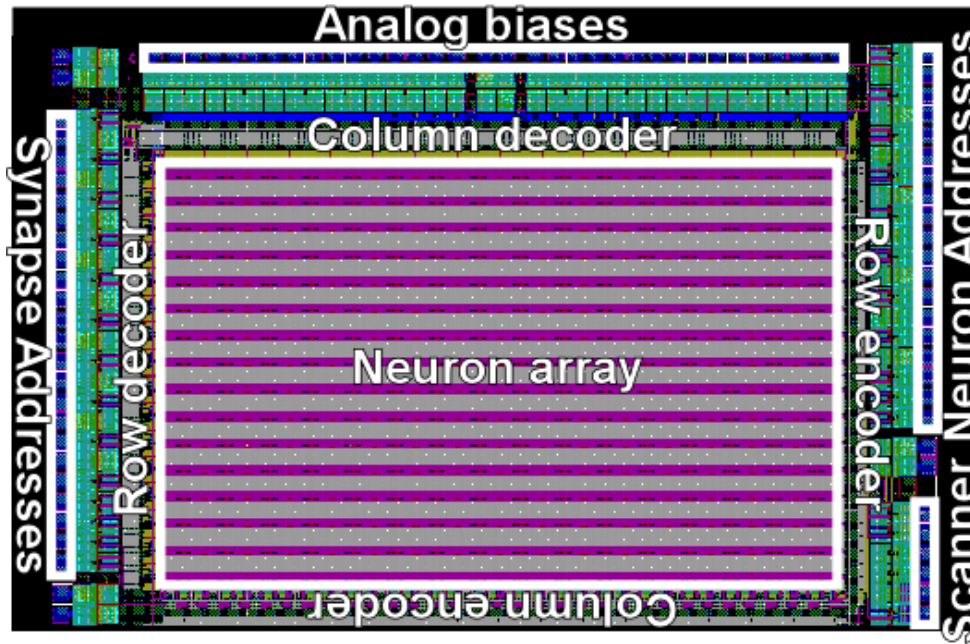
There are row and column decoders, arbiters and encoders.

Addresses specify row and column of source/target—encoded by row and column encoders and decoded by row and column decoders.

Targets can be individual STDP synapses as well as neurons, which can be excited or inhibited directly.

STDP chip's *microcircuit*
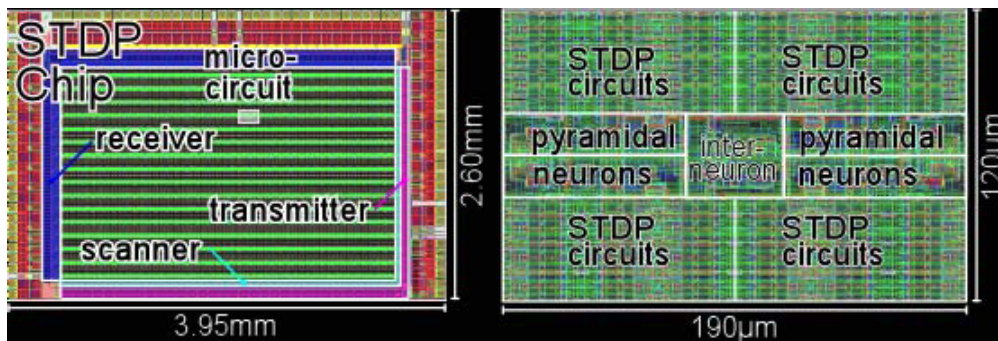
The chip's core is tiled with a regular array of identical *microcircuits.*

A microcircuit includes 4 pyramidal neurons and 1 interneuron; there are 21 plastic synapses (STDP) for each pyramidal neuron.

With a 16×16 array of microcircuits, the chip has a total of 1024 pyramidal cells, 256 interneurons, and 21,504 plastic synapses, all of which are individually addressable.
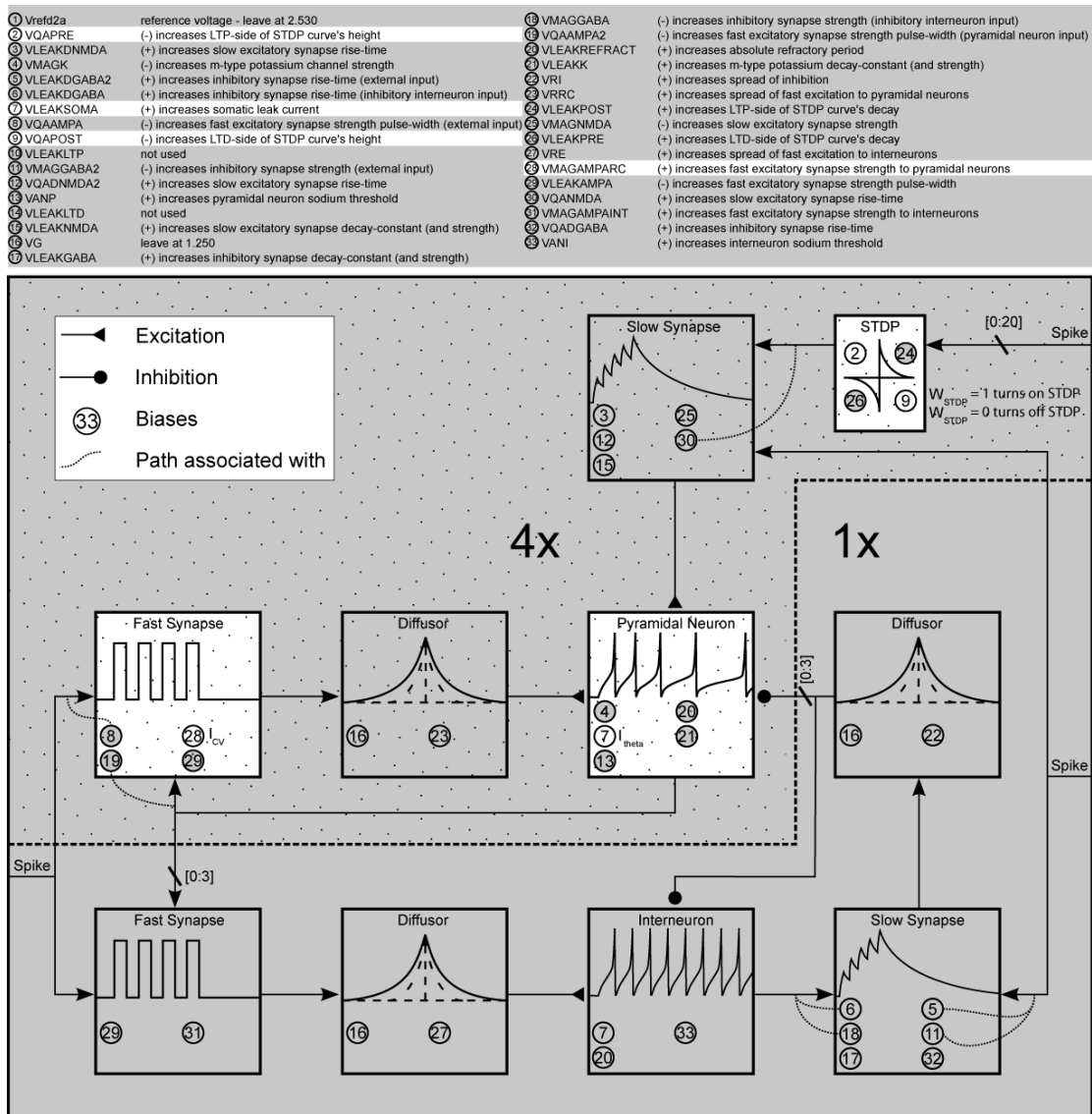
Microcircuit schematic

#	Name	Description
1	Vrefd2a	reference voltage - leave at 2.530
2	VQAPRE	(-) increases LTP-side of STDP curve's height
3	VLEAKDNMDA	(+) increases slow excitatory synapse rise-time
4	VMAGK	(-) increases m-type potassium channel strength
5	VLEAKDGABA2	(+) increases inhibitory synapse rise-time (external input)
6	VLEAKDGABA	(+) increases inhibitory synapse rise-time (inhibitory interneuron input)
7	VLEAKSOMA	(+) increases somatic leak current
8	VQAAMPA	(-) increases fast excitatory synapse strength pulse-width (external input)
9	VQAPOST	(-) increases LTD-side of STDP curve's height
10	VLEAKLTP	not used
11	VMAGGABA2	(-) increases inhibitory synapse strength (external input)
12	VQADNMDA2	(+) increases slow excitatory synapse rise-time
13	VANP	(+) increases pyramidal neuron sodium threshold
14	VLEAKLTD	not used
15	VLEAKNMDA	(+) increases slow excitatory synapse decay-constant (and strength)
16	VG	leave at 1.250
17	VLEAKGABA	(+) increases inhibitory synapse decay-constant (and strength)
18	VMAGGABA	(-) increases inhibitory synapse strength (inhibitory interneuron input)
19	VQAAMPA2	(-) increases fast excitatory synapse strength pulse-width (pyramidal neuron input)
20	VLEAKREFRACT	(+) increases absolute refractory period
21	VLEAKK	(+) increases m-type potassium decay-constant (and strength)
22	VRI	(+) increases spread of inhibition
23	VRRC	(+) increases spread of fast excitation to pyramidal neurons
24	VLEAKPOST	(+) increases LTP-side of STDP curve's decay
25	VMAGNMDA	(-) increases slow excitatory synapse strength
26	VLEAKPRE	(+) increases LTD-side of STDP curve's decay
27	VRE	(+) increases spread of fast excitation to interneurons
28	VMAGAMPARC	(+) increases fast excitatory synapse strength to pyramidal neurons
29	VLEAKAMPA	(-) increases fast excitatory synapse strength pulse-width
30	VQANMDA	(+) increases slow excitatory synapse rise-time
31	VMAGAMPAINT	(+) increases fast excitatory synapse strength to interneurons
32	VQADGABA	(+) increases inhibitory synapse rise-time
33	VANI	(+) increases interneuron sodium threshold

Pyramidal cells and interneurons intereact through fast and slow synapses and diffusors, which model their dendritic arbor's cable-like decay.
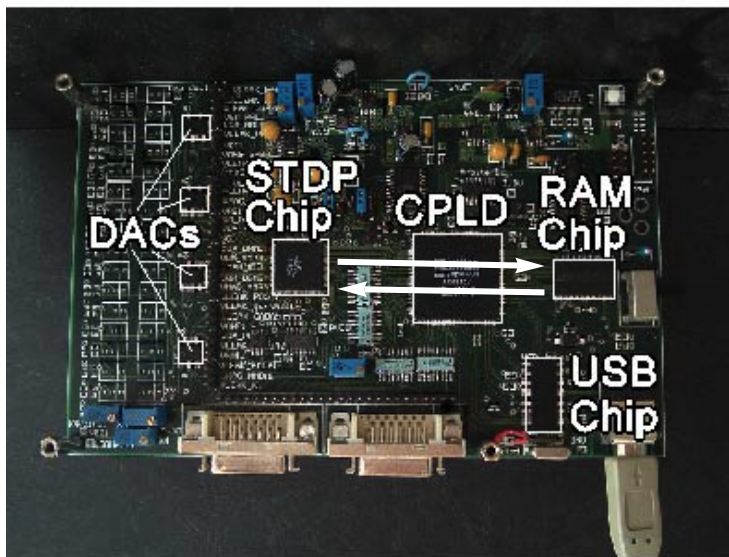
Many inputs are shared:

—Input_slow drives the slow inhibitory synapse as well as the slow excitatory synapse.

—Input_fast provides fast excitation to the pyramidal neurons as well as the interneuron.

However, the strengths of these inputs can be controlled independently.

Specifying connectivity

A look-up table is stored in the RAM.

When a pyramidal neuron spikes it can trigger up to 32 (arbitrary) synapses on the chip.